16~~22~~. (Amended) The apparatus of claim 13~~19~~, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to the switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein the switch is operative to selectively pre-charge the negative pump MOS regulation capacitors by connecting the reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance according to the pre-charge pulse signal.

REMARKS

The Office Action dated May 1, 2002 has been received and carefully reviewed. Claims 2-7, 10, 12-15, and 18-22 are currently pending in the application. Applicants note with appreciation the indication in the Office Action that claims 2-7 and 12-15 would be allowable if rewritten in independent form. In addition, Applicants note the prior art made of record and not relied upon in the Office Action. In response to the Office Action, the specification has been amended above at page 12 to more clearly refer to drawing Fig. 6 in discussing reference items 270-273 and 134a without adding new matter. In addition, claims 1, 8, 9, 11, 16, and 17 have been cancelled without prejudice or disclaimer, and claims 2, 10, 12, 18-20, and 22 have been amended, whereby the application including pending claims 2-7, 10, 12-15, and 18-22 is now believed to be in condition for allowance in view of the above amendments and the following discussion.

I. OBJECTIONS TO THE DRAWINGS.

The drawings were objected to for failing to show gates 270-273 (referenced on page 12, line 7 of the specification) and switch 134a (referenced on page 12, line 11 of the specification). Applicants note that these reference items 270-273 and 134a appear in Fig. 6 of the original drawings, and have amended the paragraph at lines 1-12

of page 12 in the specification to more clearly refer to drawing Fig. 6 in discussing reference items 270-273 and 134a without adding new matter. Accordingly, parenthetical references to Fig. 6 have been added to this paragraph where reference items 270-273 and 134a are discussed by the above amendment, whereby Applicants respectfully request withdrawal of the objection to the drawings.

II. **REJECTION OF CLAIMS 1, 8-11, and 16-22 UNDER 35 U.S.C. § 102.**

Claims 1, 8-11, and 16-22 were rejected in the Office Action under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No.5,282,170 to Van Buskirk et al. Reconsideration and withdrawal of this rejection is respectfully requested for at least the following reasons.

The Office Action indicated that claims 2-7 and 12-15 would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. By the above amendment, claims 1, 8, 9, 11, 16, and 17 have been cancelled without prejudice or disclaimer, claim 2 has been rewritten in independent form to include all of the limitations of the cancelled base claim 1, and claim 12 has been rewritten in independent form to include all of the limitations of the cancelled base claim 11. In addition, claims 10 and 18 have been amended to depend from independent claims 2 and 12, respectively, as well as to correct grammatical errors therein without adding new matter. Accordingly, claims 2-7, 10, 12-15, and 18 are now believed to be in allowable form, and notice thereof is respectfully requested.

As indicated in the Office Action, the record art does not teach a method of erasing a core memory having a pre-charge signal having a pulse duration. Accordingly, independent claim 19 and claims 20 and 22 depending therefrom have been amended to recite a pre-charge pulse signal, whereby claims 19-22 are now believed to be patentably distinct from Van Buskirk et al. Applicants therefor request reconsideration and allowance of claims 19-22 under 35 U.S.C. § 102(e).

III. CONCLUSION

For at least the above reasons, pending claims 2-7, 10, 12-15, and 18-22 currently under consideration are believed to be in condition for allowance, and notice thereof is respectfully requested.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP542US.

Respectfully submitted,
ESCHWEILER & ASSOCIATES, LLC

By _____
Thomas G. Eschweiler
Reg. No. 36,981

National City Bank Building
629 Euclid Avenue, Suite 1210
Cleveland, Ohio 44114
(216) 502-0600

CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Box Non-Fee Amendment, Assistant Commissioner for Patents, Washington, D.C. 20231.

Date: May 13, 2002 _____
Christine Gillroy

APPENDIX CONTAINING AMENDMENTS IN MARKED UP FORMAT

IN THE SPECIFICATION:

On page 12 of the application, please replace the existing paragraph at lines 1-12 with the following replacement paragraph.

--As illustrated in Fig. 7, ENPGMR going low causes PGMR to go high via gates 220, 222, 224, 226, 228, and 230, and begins a timer circuit (not shown). PGMR going high turns on switch 134a via signal VREFGATE, connecting the divider capacitors C_1 and C_2 with the voltage reference VREF, for example, about 1.3 volts. Referring also to a timing diagram 150 of Fig. 8, about 160ns after PGMR goes high, PGMR again goes low, causing a pulse signal ONESHOT 260 upon a high going pulse T1 from the timer circuit via gates 270-273 (Fig. 6). The low-going transition of PGMR causes ER_D to go high, resulting in VREFGATE going low, thereby disconnecting the reference VREF from the capacitors C_1 and C_2, once the time period (*e.g.*, about 160ns) is complete. This time period provides sufficient time for pre-charging of the negative regulation divider capacitors to allow proper regulation after switch 134a (Fig. 6) opens in the illustrated implementation of circuit 130.--

IN THE CLAIMS:

Please cancel claims 1, 8, 9, 11, 16, and 17 without prejudice or disclaimer, and amend claims 2, 10, 12, 18-20, and 22 as provided below.

1. (Cancelled)

2. (Amended) [The method of claim 1,]A method of erasing a core memory cell using a negative gate voltage in a semiconductor memory device, comprising:

generating an erase signal to begin an erase operation;

generating a pre-charge signal according to the erase signal;

pre-charging negative pump MOS regulation capacitors according to the pre-charge signal;

regulating a negative pump voltage using the pre-charged negative pump MOS regulation capacitors; and

erasing the core memory cell by applying a negative gate voltage to the core memory cell using the regulated negative pump voltage;

wherein generating a pre-charge signal comprises generating a pulse, and wherein pre-charging negative pump MOS regulation capacitors comprises connecting a reference voltage to the negative pump MOS regulation capacitors according to the pulse.

8. (Cancelled)

9. (Cancelled)

10. (Amended) The method of claim [1]2, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to a switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein pre-charging the negative pump MOS regulation capacitors comprises connecting [a]the reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance using the switch.

11. (Cancelled)

12. (Amended) [The method of claim 11,]A method of providing a negative gate voltage during a core memory cell erase operation, comprising:

generating a pre-charge signal;

pre-charging negative pump MOS regulation capacitors according to the pre-charge signal;

regulating a negative pump voltage using the pre-charged negative pump MOS regulation capacitors; and

providing a negative gate voltage to the core memory cell using the regulated negative pump voltage;

wherein generating a pre-charge signal comprises generating a pulse, and wherein pre-charging negative pump MOS regulation capacitors comprises connecting a reference voltage to the negative pump MOS regulation capacitors according to the pulse.

16. (Cancelled)

17. (Cancelled)

18. (Amended) The method of claim [11]12, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to a switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein pre-charging the negative pump MOS regulation capacitors comprises connecting [a]the reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance using the switch.

19. (Amended) An apparatus for pre-charging negative pump MOS regulation capacitors during a core cell erase operation in a memory device, comprising:

a switch connected between a reference voltage and the negative pump MOS regulation capacitors; and

a pre-charge control circuit providing a pre-charge pulse signal to the switch;

wherein the switch is operative to selectively connect the reference voltage to the negative pump MOS regulation capacitors according to the pre-charge pulse signal.

20. (Amended) The apparatus of claim 19, wherein the pre-charge control circuit receives an erase signal during the core cell erase operation, and generates the pre-charge pulse signal for a time period, and wherein the switch connects the reference voltage to the negative pump MOS regulation capacitors during the time period.

22. (Amended) The apparatus of claim 19, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to the switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein the switch is operative to selectively pre-charge the negative pump MOS regulation capacitors by connecting the reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance according to the pre-charge pulse signal.